REMARKS

Claims 1-16, all the claims pending in the application, stand rejected. In addition, claim 1 is objected to. Claims 1, 2, 4, 5 and 7-16 are amended. The amendments are intended to add further clarity and to state the claim limitations structurally, rather than functionally through a means-plus-function format.

Claim Objections

Claim 1 is objected to because the word "form" should be changed to "from." Applicant has for amended claim 1 accordingly.

Claim Rejections - 35 U.S.C. § 112

Claims 5, 10, 11, 13 and 14 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The Examiner notes that the claims recite the limitation "the multiplexer." The Examiner finds insufficient antecedent basis for this limitation in the claim. Applicant has amended the claims to provide proper antecedent basis for all claim limitations.

Claim Rejections - 35 U.S.C. § 102

Claims 1 and 4 are rejected under 35 U.S.C. § 102(b) as being anticipated by Iijima (2002/0051415). This rejection is traversed for at least the following reasons.

Independent claim 1 defines the invention as a recording pulse generator comprising several elements, all of which are now recited in structural language. With respect to the disclosed embodiment of Fig. 1, the elements of the pulse generator include "a first delay line," which corresponds to the delay line 11, having plural circuit elements cascaded in multiple stages. As now amended, the delay line outputs several "output pulses." This structure is explained at page 11 of the original application.

Claim 1 has been amended (1) to state that the delay line outputs "output signals" and (2) to state that the output signals are input to a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively." This latter feature corresponds to the parallel arrangement of inverting amplifiers, each having an output to a respective level shifter (LVS 22). As is clear from the Figure, in response to the control signal Vs that is output by the PLL oscillator 1, the plurality of fine clock signals T0-T15 are generated.

In addition, Claim 1 has been further amended to affirmatively requires a selector that "selects an arbitrary fine clock from plural fine clocks generated." This corresponds to the multiplexer 25a, as clearly explained at page 12, lines 7-10 and page 12, line 27 - page 13, line 10 of the original application. The use of a multiplexer as the "selector" is recited in dependent claims.

Finally, claim 1 has been amended to require a "recording pulse generator." The generator is operative to generate a recording pulse "on the basis of a fine clock selected." As explained at page 12, line 28 - page 14, line 3, the selected clock is input to flip-flop 25b, along with a data signal DA and an enabling signal ERA. As explained at page 13, line 11 with regard to Fig. 4, the data signal DA1 and enabling signal ERA1, an appropriate timing causes the flip-flop 1 to operate at the timing of the selected fine clock and generate a first recording pulse output (APC1).

Iijima

The Examiner notes that Iijima discloses a recording waveform generator that includes a delay line with a plurality of delay elements connected in series which receives a first clock signal, a selector for selecting one delay clock signal from the delay clock signal group and a recording waveform generation circuit 18, as illustrated in Figs. 1 and 3. Applicants assume that the Examiner considers the delay line to be element 11a and the selector to be element 12 in Fig. 1. Applicants also note that in the embodiment of Fig. 13, a phase adjustment section 40 receives a clock signal at a PLL circuit 41 and provides it to a shift register 42 and selector 43 prior to input to the delay line 11 and selector 12.

The Examiner points to the disclosure in paragraphs [0014] and [0033] as containing pertinent teachings. In particular, the Examiner points to the delay line as being an equivalent to a structure that "generates plural fine clocks." On the basis of the clarifying amendments made, which define the delay line as producing "output signals" and a "level shift stage" as producing the fine clocks, the Examiner's analysis would not be correct and, thus, the Examiner's analysis cannot support the rejection. For anticipation, the expressly stated structure and function of each limitation must be found in the prior art, expressly or inherently. In addition to the absence of the level shift stage, Applicants submit that there is no teaching that the clocks in Iijima are

"having different phase differences with a clock inputted to the first phase of the first delay line, according to the number of stages of the plural circuit elements thereof."

In short, the absence from Iijima of "a level shift stage that shifts the levels of the plural output clocks to generate plural fine clocks, respectively," as set forth in amended Claim 1, precludes anticipation. Further, such feature would not be inherent, as it would not necessarily flow from the delay line in Iijima. Accordingly, Applicants respectfully submit that Claim 1 is not anticipated under U.S.C. 102.

Claim 4

This claim specifies that the clock selection means is a multiplexer controlled by selection signals shifted in the same phase with the fine clocks. The Examiner argues that Iijima discloses a selector selecting one delay clock signal from the delay clock signal group, on the basis of the disclosure in paragraph [0014]. The Examiner states that a selector is a switch that connects to multiple lines as equivalent to a multiplexer.

Applicants respectfully submit that the claim is patentable for the reasons given for parent claim 1. Moreover, a multiplexer is expressly required and, thus, there is no basis for anticipation since no multiplexer is taught in Iijima. As already noted, the language of the claim must be found identically in the single reference for there to be anticipation. Further, there is no teaching of the function that the selection signals are shifted in the same phase with the fine clocks. Paragraph 14 makes no mention of such coordinated shifting. Thus, for many reasons, there cannot be anticipation by Iijima.

Claim Rejections - 35 U.S.C. § 103

Claims 2, 3 and 6-9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iijima as applied to claims 1 and 4, and further in view of Hayashi et al (6,493,305). This rejection is traversed for at least the following reasons.

Iijima

The Examiner notes that claims 2, 3 and 6-9 are directed to the additional structure of a PLL oscillator and an EFM clock that is inputted to a first stage of the first delay line. The Examiner asserts that Iijima discloses the PLL oscillator and a clock inputted to the first stage

but admits it does not teach the specifics of the PLL oscillator or the EFM clock that varies according to a recording speed.

Hayashi et al

The Examiner looks to Hayashi et al for a teaching of a pulse width control circuit with a PLL oscillator having a voltage control oscillator, phase comparator and low pass filter that supplies a control voltage, with a plurality of delay cells as disclosed at col. 9, line 58, 59 and Fig. 9. The Examiner further notes that the phase comparator compares the phase of oscillator output in the reference signal at col. 9, lines 48-52 and that the low pass filter of the PLL oscillator supplies a control voltage Vt according to the phase difference signal, as disclosed at col. 9, lines 52-54. The Examiner also notes that the control voltage Vt from the low pass filter is supplied to the control terminal of both delay cells and both cells have the same circuit elements and configuration, as disclosed at col. 9, lines 66-col. 10, line 5. The use of EFM clocks is noted as well. Finally, the Examiner attempts to justify the combination of Iijima and Hayashi by asserting it would have been obvious to use a PLL oscillator and delay circuit with common circuit elements in a common supply voltage as described by Hayashi in the circuit of Iijima. The motivation is to overcome sensitivity to external effects such as power fluctuations. The Examiner also asserts it would have been obvious to use EFM clock inputs because errors are reduced. Further, since disks can be played or written at different speeds, the Examiner states that EFM data needs to be written to the disk at different speeds.

No Teaching of Level Shifting Stage

Applicants respectfully submit that these assertions by the Examiner involve a clear exercise in hindsight. First, Hayashi does not remedy the significant deficiencies of Iijima as already noted.

No Combination with Specified PLL Oscillator

Claim 2 adds the "PLL oscillator" to amended Claim 1. The recited PLL oscillator controls "a power supply line" that applies a bias voltage of "a delay line". Specifically, the PLL oscillator "controls a voltage of a power supply line for the first delay line and the oscillator of the PLL oscillators according to the phase comparison result." This is not taught in either prior art reference.

An output of the PLL oscillator of Iijima implements phase control of a signal outputted from "a delay line" (Paragraphs 55, 56 and Fig. 3). Further, the output Vt of the PLL oscillator disclosed in Hayashi does not control "a voltage of a power supply line", but it is inputted to the NMOS 107 connected in series with the inverter 101 constituting a delay cell (column 10, lines 30-40 and Fig. 10). Accordingly, Iijima and Hayashi lack the disclosure of "PLL oscillator controls a voltage of a power supply line.... according to the phase comparison result", as now stated in Claim 2. As a result, even if Iijima and Hayashi are considered together, they cannot result in the configuration of the present invention as defined by amended Claim 2. Accordingly, Claim 2 should be considered patentable over the prior art.

No Motivation to Combine

As explained at page 8 of the present application with regard to the Summary of the Invention, the disclosed recording pulse generator is intended to freely vary the run length of the EFM data by means of a signal generator composed of the multiplexer and flip-flops. This way, plural signal processing may be accomplished with one delay line, by using the delay line in common and only increasing the number of the recording pulse generators, as needed. The concern in Hayashi is simply with pulse width control in the environment indicated in Fig. 3 and Fig. 8. The goal is to compensate for delay circuits that are sensitive to external effects such as power fluctuations and temperature changes, as noted by the Examiner at col. 1, lines 50-56, and to attain short pulse widths. There is no concern with generation of multiple fine clocks with different phase differences.

Because of the difference in goals between Hayashi and Iijima, contrary to the Examiner's assertion, there would be no motivation for the combination of these references in the manner suggested, particularly in a manner that attempts to duplicate the invention of the present application.

Claims 5 and 10-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Iijima and Hayashi, as applied to claims 1-4 and 6-9, and further in view of Kobayashi et al (5,818,805). This rejection is traversed for at least the following reasons.

The Examiner characterizes claims 5 and 10-16 as being drawn to a recording pulse generator where the recording pulse generation means is provided with a flip-flop circuit that

operates based on a delayed clock selected by the multiplexer. The Examiner notes that Iijima and Hayashi disclose a recording waveform generation circuit that processes data based on a delayed signal that is supplied from a selector but do not specifically teach the elements of the circuit. The Examiner points to Kobayashi for a teaching of a recording signal generating apparatus that uses a T-type flip-flop that is triggered by the output of a data selector, with reference to Fig. 16, element 18 and the disclosure at col. 12, lines 50 and 51. The Examiner notes that the data selector provides 1 of 8 delayed clock outputs to the T-type flip-flop, with reference to Fig. 16, element 10 and the disclosure at col. 12, lines 28-36.

The Examiner asserts that it would be obvious to combine the three references and, in particular to use a flip-flop to implement the function of the recording waveform generation circuit described by Iijima.

Applicants respectfully submit that Kobayashi does not remedy the deficiencies of Iijima alone or in combination with Hayashi, as already explained. Moreover, Kobayashi does not teach how and why a combination of the distinct structures of Hayashi should be inserted into the structure of Iijima. Kobayashi is merely cited for the teaching of the use of a flip-flop.

Applicant submits that it is the combination of components in these claims that results in the advantages disclosed in the application and forms the basis for the invention. It is this combination that is not taught or suggested in the prior art, other than to the Examiner's use of hindsight based on Applicant's own teachings.

In sum, on the basis of the clarifying amendments made, and the failure of the prior art to teach all of the limitations of the claims and the failure of the prior art to teach or suggest the combination of structures in the diverse references, the claims should be held patentable.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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